Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (canceled) An apparatus comprising:

first and second bus interface circuits to interface to first and second buses, respectively, the first bus being accessible to a first processor;

a processor interface circuit to interface to a second processor, the second processor having accessibility to the first and second buses; and

an arbitration logic circuit coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first and second processors.

2. (currently amended) The apparatus of claim [[1]] 4 wherein the second processor is coupled to the first and second buses.

3. (original) The apparatus of claim 2 wherein the processor interface circuit comprises:

a command decoder to decode an access command from the second processor requesting access to one of the first and second buses.

4. (currently amended) ~~The~~ An apparatus ~~of claim 1~~ comprising:

first and second bus interface circuits to interface to first and second buses, respectively, the first bus being accessible to a first processor;

a processor interface circuit to interface to a second processor, the second processor having accessibility to the first and second buses; and

an arbitration logic circuit coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first and second processors; wherein the arbitration logic circuit disables the first bus interface circuit when the second processor requests access to the second bus.

5. (currently amended) The apparatus of claim [[1]] 4 wherein the arbitration logic circuit enables the first and second bus interface circuits when access request to the second bus from the first processor is granted.

6. (currently amended) The apparatus of claim [[1]] 4 wherein the arbitration logic circuit resolves access requests from the first and second processors such that the first processor accesses the first bus while the second processor accesses the second bus.

7. (currently amended) The apparatus of claim [[1]] 4 wherein the first processor is one of a microprocessor, a micro-controller, and a digital signal processor.

8. (currently amended) The apparatus of claim [[1]] 4 wherein the second processor is a direct memory access (DMA) controller.

9. (currently amended) The apparatus of claim [[1]] 4 wherein the first and second buses are of same type.

10. (currently amended) The apparatus of claim [[1]] 4 wherein the first and second buses are of different types.

11. (canceled) A method comprising:

interfacing to first and second buses by first and second interface circuits, respectively, the first bus being accessible to a first processor;

interfacing to a second processor, the second processor having accessibility to the first and second buses; and

arbitrating access requests from the first and second processors.

12. (currently amended) The method of claim [[11]] 14 wherein the second processor is coupled to the first and second buses.

13. (original) The method of claim 12 wherein interfacing to the second processor comprises:

decoding an access command from the second processor requesting access to one of the first and second buses.

14. (currently amended) ~~The~~ A method ~~of claim 11~~ comprising:

interfacing to first and second buses by first and second interface circuits, respectively, the first bus being accessible to a first processor;

interfacing to a second processor, the second processor having accessibility to the first and second buses; and

arbitrating access requests from the first and second processors; wherein arbitrating access requests comprises disabling the first bus interface circuit when access request to the second bus from the second processor is granted.

15. (currently amended) The method of claim [[11]] 14 wherein arbitrating access requests comprises enabling the first and second bus interface circuits when access request to the second bus from the first processor is granted.

16. (currently amended) The method of claim [[11]] 14 wherein arbitrating access requests comprises resolving the access requests from the first and second processors such that the first processor accesses the first bus while the second processor accesses the second bus.

17. (currently amended) The method of claim [[11]] 14 wherein the first processor is one of a microprocessor, a micro-controller, and a digital signal processor.

18. (currently amended) The method of claim [[11]] 14 wherein the second processor is a direct memory access (DMA) controller.

19. (currently amended) The method of claim [[11]] 14 wherein the first and second buses are of same type.

20. (currently amended) The method of claim [[11]] 14 wherein the first and second buses are of different types.

21. (canceled) A system comprising:

first and second buses;

first and second processors, the first processor being coupled to the first bus;

a bus controller coupled to the first and second buses to control bus access from the first and second processors, the bus controller comprising:

first and second bus interface circuits to interface to the first and second buses, respectively,

a processor interface circuit to interface to the second processor, the second processor having accessibility to the first and second buses, and

an arbitration logic circuit coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first and second processors.

22. (currently amended) The system of claim ~~21~~ 24 wherein the second processor is coupled to the first and second buses.

23. (original) The system of claim 22 wherein the processor interface circuit comprises:

a command decoder to decode an access command from the second processor requesting access to one of the first and second buses.

24. (currently amended) ~~The~~ A system ~~of claim 21~~ comprising:

first and second buses;

first and second processors, the first processor being coupled to the first bus;

a bus controller coupled to the first and second buses to control bus access from the first and second processors, the bus controller comprising:

first and second bus interface circuits to interface to the first and second buses, respectively,

a processor interface circuit to interface to the second processor, the second processor having accessibility to the first and second buses, and

an arbitration logic circuit coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first and second processors; wherein the arbitration logic circuit disables the first bus interface circuit when the second processor requests access to the second bus.

25. (currently amended) The system of claim ~~21~~ 24 wherein the arbitration logic circuit enables the first and second bus interface circuits when access request to the second bus from the first processor is granted.

26. (currently amended) The system of claim ~~21~~ 24 wherein the arbitration logic circuit resolves access requests from the first and second processors such that the first processor accesses the first bus while the second processor accesses the second bus.

27. (currently amended) The system of claim ~~21~~ 24 wherein the first processor is one of a microprocessor, a micro-controller, and a digital signal processor.

28. (currently amended) The system of claim ~~21~~ 24 wherein the second processor is a direct memory access (DMA) controller.

29. (currently amended) The system of claim ~~21~~ 24 wherein the first and second buses are of same type.

30. (currently amended) The system of claim ~~21~~ 24 wherein the first and second buses are of different types.